Power Combining Port Impedance Model

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Abstract:

A novel way to characterize the port impedances of broadband combining networks has been developed. The impedance of a coupler port in the environment of a fully driven combiner is analyzed to develop a thorough understanding of the interaction of power MMICs and combiners in actual manufacturing environments.

Introduction:

High power solid state generation at microwave frequencies is achieved through combining several high power GaAs MMICs. These combining techniques have been demonstrated for both distributed T/R module applications, as well as centralized transmitter applications. The combining techniques range from corporate to serial and encompass microstrip for relatively low power and waveguide for high power applications. The different techniques have been successfully modeled through Libra linear analysis and various two and three dimensional modeling tools such as Sonnet, HFSS, and Momentum. These tools have demonstrated sufficient correlation of measured to modeled combiner results for narrow band applications, i.e., less than 20% bandwidth, but lack sufficient correlation for wider band applications. This insufficient correlation represents the use not the capability of the tools. The port impedance model utilizes the same fundamental modeling tools but derives a thorough analysis of the combining structure in the environment presented to actual high power MMICs.

Port Impedance Model Description:

The port impedance model describes the impedance that an amplifying MMIC sees in the combining environment. In particular, the port impedances of the coupler structure are analyzed under the real drive conditions set up by all the amplifier MMICs working into the coupler. This technique is in contrast to the more conventional technique of modeling a single port of a coupling structure with 50 ohm terminations at the other coupler ports. The port impedance can then be used to evaluate the performance and reliability of the MMICs. These evaluations take the form of MMIC load pull data to ensure adequate power performance and time domain analysis to ensure adequate voltage break down margin.

Traditional modeling techniques investigated the passive coupler as a separate entity from the active MMICs. The couplers were modeled back-to-back in a S-parameter simulator such as Libra. The combining loss for the coupler was then taken as just half of the back-to-back insertion loss. The coupler port impedances were evaluated, one port at a time, with 50 ohm terminations at the other ports. This modeling technique proved adequate for narrow band coupling structures with good isolation, well matched termination resistors, and balanced input ports.

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The port impedance technique models the coupler in the actual amplifier environment. This model is accomplished by creating a Libra file with the back-to-back splitter and combiner couplers. One port of the combiner is then disconnected from the splitter, while leaving all of the adjacent ports connected. The open port on the splitter is terminated in 50 ohms. The adjacent port of the combiner is fed by an ideal coupler with a time delay equivalent to the terminated splitter path. The ideal coupler simultaneously feeds the output combiner port and the input of the back-to-back coupler structure. This effectively drives all ports of the back-to-back couplers while evaluating a single coupling port. The block diagram for the port impedance model is shown in Figure 1. An ideal isolator is placed in front of the splitter to isolate the return loss of the splitter input for the combiner test port.

Once the basic port impedance model is set, S-parameter files are added between adjacent splitter combiner ports to simulate fully driven power amplifier MMIC. A saturated amplifier effect is accomplished by editing the S-parameter file to make all of the insertion losses the same. This ensures all of the combiner ports will be driven by the same amplitude. The S-parameter file also incorporates the power MMIC isolation and large signal output impedance characteristics. These S-parameter characteristics are required to show the impact of adjacent ports on the test port.

The port impedance model is then altered to show the effects of non-ideal phase and amplitude imbalances. The effect of non-ideal termination resistors on the couplers shows the sensitivity of the loads on the port impedance. This effect becomes more prevalent with greater port to port amplitude and phase imbalances. Manufacturing variations such as chip placement, wire bond lengths, coupler line widths, and dielectric material variations are also accounted for in the model. All of these

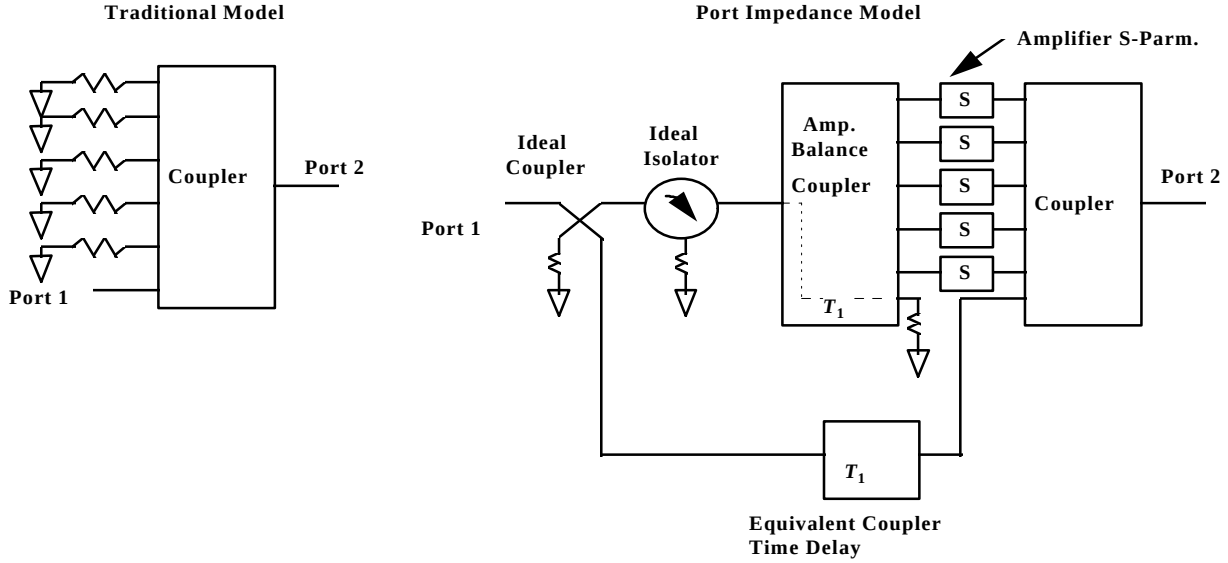

Figure 1 Port Impedance Block Diagrams

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variations are first modeled in a 3-dimensional simulator such as HFSS. Their S-parameter files are imported into the Libra model to study their effect and sensitivity on port impedance.

This new way of modeling the port impedance evaluates the effects of finite coupler isolation, amplitude imbalances to the output coupler created by the saturation effects of the amplifiers, return losses of the amplifiers, non ideal termination resistors, and manufacturing variations. These effects become increasingly important with wider bandwidth circuit designs.

Results:

This modeling technique was successfully utilized on a 6 way power combiner with greater than 60% bandwidth at X-band. The block diagram and picture of the power amplifier with the 6-way combiner, 6-way splitter and power MMICs are shown in Figure 2a and 2b. The 6-way

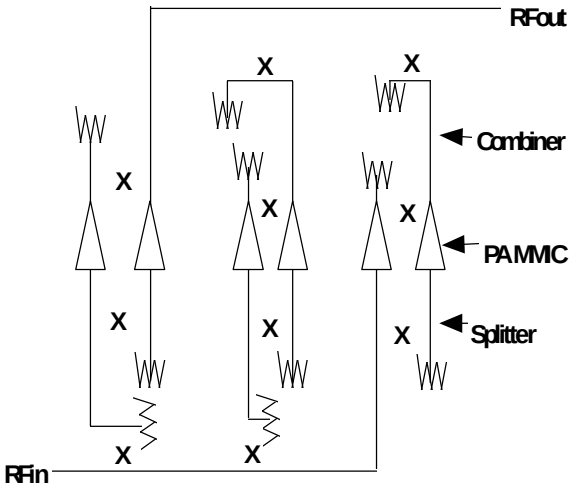

Figure 2a Power Amplifier Block Diagram

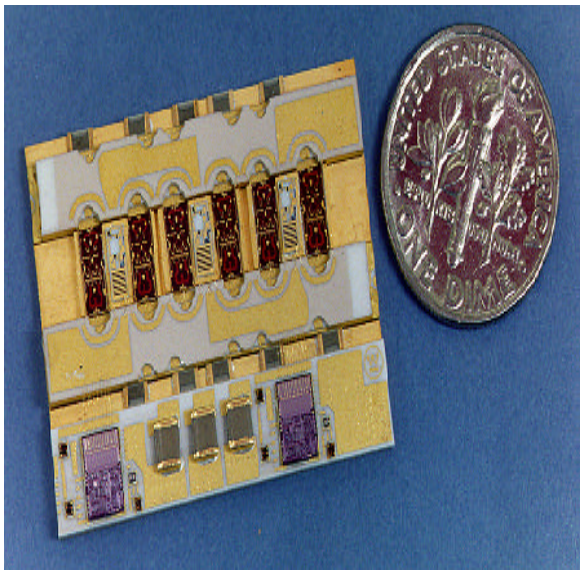

Figure 2b Power Amplifier

power combiner was comprised of 3 identical 2-way corporate couplers followed by a 3-way serial coupler. The couplers were implemented in stripline overly geometrics. The port impedances were evaluated and used to determine the output power variation of the overall power amplifier due to load pull effects. The model outputs were also used to determine safe operating bias points to maintain dynamic voltage swings away from breakdown.

These model outputs are shown in Figure 3, highlighting the traditional model port impedance and the new modeled port impedance for the 6 ports. The traditional model shows port impedances with VSWRs less than 1.5:1. The port impedance model shows port impedances with VSWRs less than 2.5:1. This increase in VSWR resulted in a power loss of 0.3 dB over what the traditional model predicted.

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Traditional Model **Port Impedance Model**

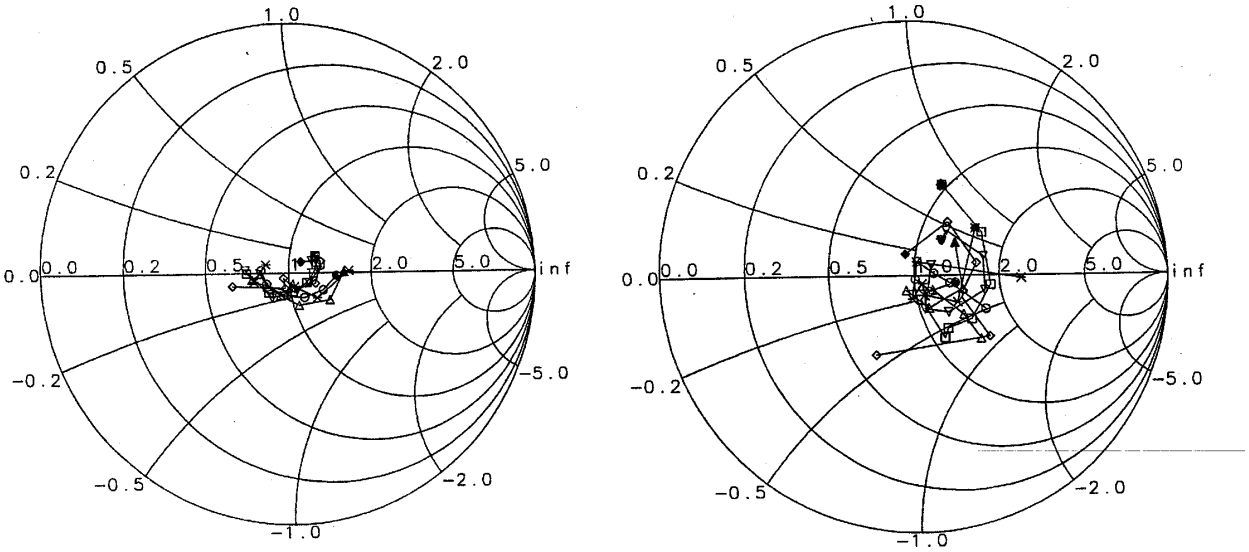

Figure 3 Port Impedance for Models